Precision 3-Channel Delay Generator DLY3CH 1.0a

Developer's Guide

PRELIMINARY
INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE WITHOUT NOTIFICATION

Chapter 1 Introduction to the DLY3CH

OVERVIEW

The Raptor Engineering Precision 3-Channel Delay Generator [DLY3CH] is a high performance 2.2ns-12.2ns independent delay generator. This board utilizes three Micrel 100EP196VTG precision delay generators, and can adjust each channel's delay in +/-10ps increments. Additionally, a +/-30ps analog fine tuning control is provided on each channel to allow for precise edge synchronization in almost any application. To align input clock edges, the RF input to each delay generator is registered, and a single RF clock input clocks each of the three input registers.

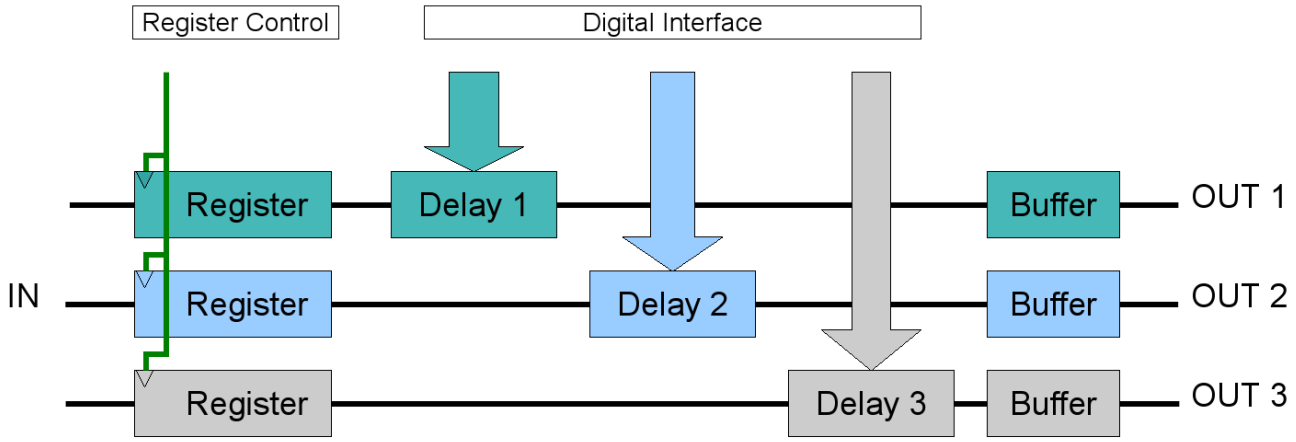
The DLY3CH can be readily used with any FPGA that makes a Digilent-compatible 40-pin expansion header available, such as the Raptor Engineering VDFPGA series of development boards. Two 11-bit and one 8-bit LVCMOS/LVTTL digital delay control inputs are available; one for each delay channel. All clock inputs and outputs are LVTTL/LVCMOS compatible, and the output header is pin compatible with the Raptor Engineering Triple RF Generator [CERFBOARD].

A typical application for this board combined with the CERFBOARD would be a small linear particle accelerator, to provide the required adjustable precision delays to the individual accelerating elements from the incoming RF master clock(s).

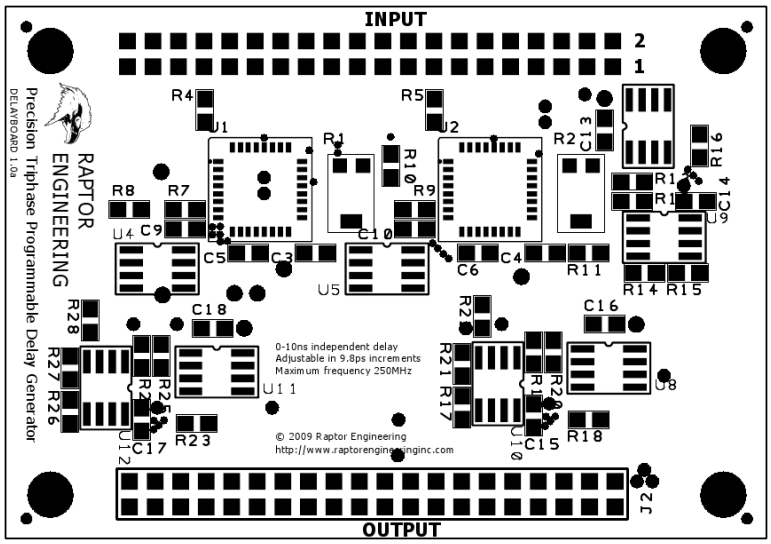
The digital protocol used by the digital delay inputs is described in detail by the Micrel 100EP196VTG public datasheet, which is available for download on the Raptor Engineering website.

Please note that delay channel 1 only allows 2.2ns-4.3ns delay adjustment, due to the limited number of pins on the control header. Also, due to the nature of the delay circuitry, this board will consume a moderately high amount of power, and heat up significantly during operation. This is normal, and will not adversely affect the operation or lifespan of the DLY3CH board in any way.

BLOCK DIAGRAM



HARDWARE



Interface Header Pin Number:	Pin Description:	Interface Header Pin Number:	Pin Description:
1	DGND [PASSTHROUGH]	21	Channel 1 Data Bit 5
2	+5.0V [PASSTHROUGH]*	22	Channel 1 Data Bit 6
3	+3.3V [PASSTHROUGH]	23	Channel 1 Data Bit 3
4	Channel 1 Control Latch	24	Channel 1 Data Bit 4
5	Channel 2 RF In	25	Channel 3 Data Bit 0
6	Channel 3 RF In	26	Channel 1 Data Bit 2
7	Channel 2 Data Bit 0	27	Channel 3 Data Bit 2
8	Channel 1 RF In	28	Channel 3 Data Bit 1
9	Channel 2 Data Bit 2	29	Channel 3 Data Bit 4
10	Channel 2 Data Bit 1	30	Channel 3 Data Bit 3
11	Channel 2 Data Bit 4	31	Channel 3 Data Bit 6
12	Channel 2 Data Bit 3	32	Channel 3 Data Bit 5
13	Channel 2 Data Bit 6	33	Channel 3 Control Latch
14	Channel 2 Data Bit 5	34	Channel 3 Data Bit 7
15	Channel 2 Control Latch	35	Channel 3 Data Bit 9
16	Channel 2 Data Bit 7	36	Channel 3 Data Bit 8
17	Channel 2 Data Bit 9	37	Channel 1 Data Bit 1
18	Channel 2 Data Bit 8	38	Channel 3 Data Bit 10
19	Channel 1 Data Bit 7	39	Shared RF Register Clock
20	Channel 2 Data Bit 10	40	Channel 1 Data Bit 0

* This signal is not required for proper operation of the DLY3CH board, but is simply connected to the identical pin on the output header as a convenience.

DLY3CH UCF for Raptor Engineering® VDFPGA Development Board [40-pin Connectors]:

```
NET channel1_len LOC=A20;
NET channel1_lf_in LOC=D18;
NET channel1_data<0> LOC=U21;
NET channel1_data<1> LOC=V11;
NET channel1_data<2> LOC=J22;
NET channel1_data<3> LOC=G22;
NET channel1_data<4> LOC=H22;
NET channel1_data<5> LOC=F22;
NET channel1_data<6> LOC=F20;
NET channel1_data<7> LOC=E22;

NET channel2_len LOC=C21;
NET channel2_lf_in LOC=B20;
NET channel2_data<0> LOC=C18;
NET channel2_data<1> LOC=A17;
NET channel2_data<2> LOC=B17;
NET channel2_data<3> LOC=C19;
NET channel2_data<4> LOC=A18;
NET channel2_data<5> LOC=B22;
NET channel2_data<6> LOC=B21;
NET channel2_data<7> LOC=C22;
NET channel2_data<8> LOC=D22;
NET channel2_data<9> LOC=D21;
NET channel2_data<10> LOC=E20;

NET channel3_len LOC=P22;
NET channel3_lf_in LOC=D17;
NET channel3_data<0> LOC=G20;
NET channel3_data<1> LOC=L22;
NET channel3_data<2> LOC=K22;
NET channel3_data<3> LOC=N21;
NET channel3_data<4> LOC=M22;
NET channel3_data<5> LOC=P20;
NET channel3_data<6> LOC=N22;
NET channel3_data<7> LOC=R22;
NET channel3_data<8> LOC=E12;
NET channel3_data<9> LOC=R21;
NET channel3_data<10> LOC=T22;

NET hf_clock_in LOC=U22;
```

DLY3CH UCF for Digilent® Spartan-3 Development Board [B1 Connector]:

```
NET channel1_len LOC=C10;
NET channel1_lf_in LOC=C11;
NET channel1_data<0> LOC=M11;
NET channel1_data<1> LOC=R14;
NET channel1_data<2> LOC=E16;
NET channel1_data<3> LOC=D15;
NET channel1_data<4> LOC=D16;
NET channel1_data<5> LOC=C15;
NET channel1_data<6> LOC=C16;
NET channel1_data<7> LOC=M6;

NET channel2_len LOC=R7;
NET channel2_lf_in LOC=T3;
NET channel2_data<0> LOC=N11;
NET channel2_data<1> LOC=D11;
NET channel2_data<2> LOC=P10;
NET channel2_data<3> LOC=C12
NET channel2_data<4> LOC=R10;
NET channel2_data<5> LOC=D12;
NET channel2_data<6> LOC=T7;
NET channel2_data<7> LOC=E11;
NET channel2_data<8> LOC=B16;
NET channel2_data<9> LOC=N6;
NET channel2_data<10> LOC=R3;

NET channel3_len LOC=K16;
NET channel3_lf_in LOC=E10;
NET channel3_data<0> LOC=E15;
NET channel3_data<1> LOC=G15;
NET channel3_data<2> LOC=F15;
NET channel3_data<3> LOC=H15;
NET channel3_data<4> LOC=G16;
NET channel3_data<5> LOC=J16;
NET channel3_data<6> LOC=H16;
NET channel3_data<7> LOC=K15;
NET channel3_data<8> LOC=B3;
NET channel3_data<9> LOC=L15;
NET channel3_data<10> LOC=N9;

NET hf_clock_in LOC=T15;
```

If you encounter any hardware problems, please contact us at support@raptorengineeringinc.com.

Raptor Engineering

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Designed and manufactured in the U.S.A.
