VDCAM Bus Specification

Revision 1.0a

PRELIMINARY
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Chapter 1 Bus Signals

FALCON MODULE BUS

The FALCON Module Bus is a synchronous, single master bus with clock and memory signals.
The bus may be expanded with additional data vectors as needed.
All vectors shown below are optional, with the exception of enable and done.

Signal Name	Width	Direction	Polarity	Description
address	20	Out	Active High	RAM address
data_write	32	Out	Active High	Data to write to RAM
data_read	32	In	Active High	Data read from RAM
wren	1	Out	Active High	RAM write enable
data_read_offset	20	In	Active High	Memory read offset address
data_write_offset	20	In	Active High	Memory write offset address
enable	1	In	Active High	Enable processing operations All other modules have released RAM control
done	1	Out	Active High	Signal that processing is complete RAM control must be released at this time
clk	1	In	Active High	25MHz clock input
clk_inv	1	In	Active High	25MHz inverted clock input
hundred_clk	1	In	Active High	100MHz clock input
hundred_clk_inv	1	In	Active High	100MHz inverted clock input

TIMING DIAGRAM LEGEND

tAS	Window after positive edge of clk during which address must become valid
tWE	Window after positive edge of clk during which wren must become valid
tDS	Window after positive edge of clk during which data_write must become valid

MODULE TIMING REQUIREMENTS

tAS	≤ 11ns
tWE	≤ 13ns
tDS	≤ 24ns

FALCON BLOCK BUS

The FALCON Block Bus is a high-speed synchronous, point to point bus with clock and memory.
The bus may be expanded with additional data vectors as needed.
All vectors shown below are optional, with the exception of enable and done.

Signal Name	Width	Direction	Polarity	Description
address	10	Out	Active High	RAM address
data_write	32	Out	Active High	Data to write to RAM
data_read	32	In	Active High	Data read from RAM
wren	1	Out	Active High	RAM write enable
subprocess_enable	1	In	Active High	Enable processing operations All other modules have released RAM control
subprocess_done	1	Out	Active High	Signal that processing is complete RAM control must be released at this time
patch_dimension	16	Out	Active High	The X and Y pixel dimension of each block that will be extracted from the main image.
clk	1	In	Active High	100MHz clock input

Chapter 2 Timing Diagrams

FALCON MODULE BUS

This diagram illustrates a typical module enable/disable sequence, with a module executing a single read and write to external RAM. Most modules will execute many thousands of RAM read and write operations before enabling the done signal.

FALCON BLOCK BUS

This diagram illustrates a typical module enable/disable sequence, with a module executing a two reads and a single write to external RAM. Most modules will execute many thousands of RAM read and write operations before enabling the done signal.

Chapter 3 Related Information

Related Resources
Additional documentation on the VDCAM Reference Design is available here:
http://www.raptorengineeringinc.com/content/VDCAM/sintro.html

Specification Availability
The VDCAM Reference Design is available for all Raptor Engineering FPGA development systems. Additionally, any modules created conforming to the above specification are guaranteed to interface with any Raptor Engineering product compliant with version 1.0a of the VDCAM bus specification.

Support
For hardware or software support, please contact us at support@raptorengineeringinc.com.

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